Register Number:……..

KUMARAGURU
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B.E/B.TECH DEGREE EXAMINATIONS: NOV/DEC 2024

(Regulation 2018)

Third Semester

COMPUTER SCIENCE AND ENGINEERING

U18CST3003: Computer Architecture

COURSE OUTCOMES

CO1: Identify the different addressing modes used in a processor.
CO2: Apply the knowledge of arithmetic operations in the design of a fast adder.
CO3: Classify the control units present in a processor.
CO4: Analyze the various performance enhancement techniques of cache memories.

CO5: Point out how the pipeline processor improves performance of a computer.

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-
PART A (10 x 2 = 20 Marks)
(Answer not more than 40 words)

1.	Define addressing modes and explain the purpose of using different addressing modes in a processor.	CO1	[K_2]
2.	Discuss the significance of bus structure in computer architecture.	CO1	[K_2]
3.	Explain how signed numbers are represented using two's complement notation.	CO2	[K_2]
4.	Narrate the steps involved in storing a word in memory from a processor register.	CO3	[K_2]
5.	Define cache memories and how do they enhance the performance of a computer system?	CO4	[K_2]
6.	Explain the concept of instruction pipelining and its impact on processor performance.	CO5	[K_2]
7.	Given an example, describe how data hazards can occur in a pipelined processor.	CO5	[K_2]
8.	Calculate the effective address in indexed addressing mode if the base address is 3000 and the index register contains 50.	CO1	[K_3]
9.	List and briefly explain any two types of interrupts in computer systems.	CO3	[K_2]
10.	Analyze the impact of increasing cache block size on hit rate and miss penalty.	CO5	[K_2]

Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11. Scenario: A financial institution requires a custom arithmetic unit capable of performing high-speed calculations for complex financial models. The unit must handle large numbers with precision and support operations like addition, subtraction, multiplication, and division of both integers and floating-point numbers.
Specific Details:
- The arithmetic unit should efficiently add and subtract large signed integers.
- Multiplication and division operations must be optimized for speed.
- Floating-point operations should comply with IEEE 754 standard.
- The design should balance performance with cost-effectiveness.

a)	Design a fast adder suitable for adding large signed integers. Explain the working of a carry-lookahead adder and how it improves speed over a ripple-carry adder.	7	CO2	[K_4]
b)	Propose an algorithm or hardware design for fast multiplication of signed numbers.	7	CO2	[K_4]
c)	Why is adherence to the IEEE 754 standard crucial in floating-point arithmetic for financial calculations?	2	CO2	[K_2]

12. Scenario: A gaming company aims to enhance the performance of its gaming console without significant hardware upgrades. The focus is on improving processor speed, reducing latency, and handling complex graphics efficiently.
Specific Details:
- The current processors suffer from frequent pipeline stalls due to data hazards.
- Cache memory performance is suboptimal, leading to slow game loading times.
- There are bottlenecks in I/O operations affecting real-time gaming experiences.
- Budget constraints limit extensive hardware modifications.

a)	Analyze techniques to improve cache memory performance, such as increasing associativity, implementing cache replacement policies, or using write-back caches.	7	CO4	[K_4]
b)	Discuss methods to minimize pipeline hazards, including data forwarding and instruction reordering. Explain how these methods can be applied to enhance processor performance in the gaming console.	7	CO5	[K_3]
c)	Explain how implementing Direct Memory Access (DMA) can alleviate I/O bottlenecks in the gaming console.	2	CO5	[K_2]

13.	a)	Describe at least four different addressing modes used in processors. Provide assembly language examples for each.	7	CO1	[K_3]
	b)	Given the instruction LOAD R1, 1000(R2), where R2 contains the value 2000, calculate the effective address and explain how the processor fetches the data using indexed addressing mode.	7	CO1	[K_3]
	c)	How do addressing modes enhance the flexibility of programming in assembly language?	2	CO1	[K_2]
14.	a)	Explain the differences between hardwired and microprogrammed control units. Discuss the advantages and disadvantages of each type.	7	CO3	[K_4]
	b)	Describe the structure of a microprogrammed control unit, including control memory, microinstruction formats, and microinstruction sequencing.	7	CO3	[K_2]
	c)	In what scenarios would a microprogrammed control unit be preferred over a hardwired control unit?	2	CO3	[K_2]
15.	a)	Discuss the factors that affect cache performance, including cache size, block size, associativity, and replacement policies. Analyze how each factor influences hit rate and system performance.	7	CO4	[K_4]
	b)	A processor has a cache memory of 32KB with a block size of 64 bytes and uses 8-way set associativity. Calculate the number of sets in the cache and explain the mapping process of memory addresses to cache lines.	7	CO4	[K_3]
	c)	Differentiate between volatile and non-volatile memory systems.	2	CO4	[K_2]
16.	a)	Illustrate the concept of instruction pipelining with a diagram of a 5-stage pipeline. Explain each stage and how pipelining increases instruction throughput.	7	CO5	[K_3]
	b)	Identify and explain the three types of hazards in pipelined processors: structural, data, and control hazards. Provide strategies to overcome each type.	7	CO5	[K_3]
	c)	Assess the impact of branch prediction on pipeline performance.	2	CO5	[K_4]

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