Register Number:……..

B.E DEGREE EXAMINATIONS: NOV/DEC 2024

(Regulation 2018)

Seventh Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U18ECE0043**:** System on Chip

COURSE OUTCOMES

CO1: Discuss system architectures and components.

CO2: Outline system level design methodology.

CO3: Compare hardware software co design strategies.

CO4: Illustrate SOC design approach.

CO5: Discuss SOC design implementation tools.

CO6: Summarize SOC testing techniques.

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions:-

PART A (10 x 1 = 10 Marks)

1. Match the given pipelined processors (List –I) with their number of instructions decoded per cycle (List-II) CO1 [K_2]

List I (Processors)	**List II (Number of Instructions per cycle)**
A. Partial or Static Pipeline	i. 4
B. Superscalar Processors	ii. 1
C. VLIW processors	iii. 1 or less
D. Out- of Order pipeline	iv. 8

	A	B	C	D
a)	ii	i	iii	iv
b)	iii	iv	ii	i
c)	ii	iv	iii	i
d)	iii	i	iv	ii

2. Identify the module : It is a simple register system, containing 64 and 256 entries, used to save recent address translations for reuse. CO2 [K_2]

a) Translational Look Ahead Buffer
b) External Memory
c) Cache Memory
d) Shift Register

3. The IEEE 1500 std is a CO6 [K_2]

1. Test Pattern
2. Test Access Mechanism (TAM)
3. Test Interface
4. Test Vector

a) Only 1
b) Only 2
c) 1,4
d) 2,3

4. The Block RAM (BRAM) in FPGA is a CO4 [K_2]

a) LIFO -Last In First Out Memory
b) FIFO – First in First Out Memory
c) FILO – First in Last Out Memory
d) LILO – Last In Last Out Memory

5. Assertion (A): The Wishbone bus-based on-chip communication architecture standard is an open-source standard. CO2 [K_2]

Reason (R): The Wishbone interface is highly configurable, and allows a user to customize tags or signals to support specific application requirements

a) Both A and R are Individually true and R is the correct explanation of A
b) Both A and R are Individually true but R is not the correct explanation of A
c) A is true but R is false
d) A is false but R is true

6. Match the family to which the ZYNQ 7000 belongs to? CO5 [K_1]

a) MCU(Micro Controller Unit)
b) MPSoC(Multi Processor SoC)
c) PSoC(Programmable SoC)
d) APSOC (All Programmable SoC)

7. Arrange the given VLSI technologies in the Decreasing order of their peak performance. Peak performance is defined as number of operations per watt. CO1 [K_2]

1. CGRA – Coarse grained Reconfigurable Architecture
2. GPP – General Purpose Processors
3. FPGA – Field Programmable Gate Array
4. ASIC – application specific Integrated Circuits

a) 2-3-4-1
b) 4-1-3-2

c) 3-4-2-1 d) 1-3-2-4

8. Identify the IEEE floating point standard supported by Microblaze processor CO4 [K_2]

a) IEEE 745 b) IEEE 724

c) IEEE 754 d) IEEE 735

9. Examine the two statements carefully and select the answer using the codes given below: CO2 [K_2]

Assertion A: On-chip peripheral bus is a synchronous bus used to connect high latency peripherals.

Reason R: OPB alleviates the system performance bottle necks by increasing the capacitive loading on the PLB.

a) Both A and R are Individually true and R is the correct explanation of A

b) Both A and R are Individually true but R is not the correct explanation of A

c) A is true but R is false

d) A is false but R is true

10. The word 'co' in the co-design concept implies CO3 [K_2]

a) Concurrent, Covariant, Compilation, Complexity

b) Coordination, Convenient, concurrency, correctness

c) Coordination, Complexity, Concurrency, Correctness

d) Coordination, Condition, Covariant, Concurrent

PART B (10 x 2 = 20 Marks)

(Answer not more than 40 words)

11. List the benefits of including memory with the processor on the die. CO1 [K_1]
12. Classify the different types of design associated with various stages of the design process in SOC design effort? CO1 [K_2]
13. What are data Interlocks? CO2 [K_1]
14. Summarize the various System Level issues and specifications to be considered while choosing a suitable interconnect for SOC architecture. CO2 [K_2]
15. Outline the driving factors in hardware/software codesign. CO3 [K_2]
16. Recall Amdahl's supercomputing law CO4 [K_1]
17. Summarize the various Abstraction levels of hardware/software codesign CO4 [K_2]
18. Outline the basic design flow for Zynq SOC. CO5 [K_2]
19. List the various issues in SoC testing. Define the terms access, control and isolation with respect to testing CO6 [K_1]

20.		What are the different TAM(Test Access Mechanism) implementation schemes?		CO6	[K_1]

Answer any FIVE Questions:-

PART C (5 x 14 = 70 Marks)

(Answer not more than 350 words)

21.	a)	Explain in detail the different classes of SIMD processor architectures with necessary block diagram.	7	CO1	[K_2]
	b)	Illustrate the memory considerations and addressing techniques that should be applied in the SoC design approach.	7	CO1	[K_2]
22.		Illustrate the principle behind Vector processors and Vector instruction extensions with suitable diagrams.	14	CO2	[K_2]
23.		Explain the various flow control schemes utilized in NOC(Network On- chip) based communication architectures	14	CO2	[K_2]
24.	a)	Demonstrate the various considerations to be accounted in hardware/software co-design space.	7	CO4	[K_2]
	b)	Summarize the concepts of dataflow modeling in hardware/software co- design.	7	CO4	[K_2]
25.		Explain the Microblaze processor architecture and Instruction set in detail with suitable diagrams.	14	CO5	[K_2]
26.		Illustrate the concepts involved in IEEE P1500 SOC testing standard with necessary diagrams	14	CO6	[K_2]

****