KUMARAGURU
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B.E/B.TECH DEGREE EXAMINATIONS: NOV/DEC 2024

(Regulation 2018)

Sixth Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U18ECE0045: Low Power VLSI

COURSE OUTCOMES

CO1: Discuss the sources of power dissipation in CMOS logic design.

CO2: Illustrate low power design and optimization techniques.

CO3: Estimate power at different levels.

CO4: Examine leakage reduction techniques.

CO5: Analyze the effects of voltage scaling.

CO6: Discuss effect of capacitance on power reduction.

Time: Three Hours   **Maximum Marks: 100**

Answer all the Questions:-
PART A (10 x 2 = 20 Marks)
(Answer not more than 40 words)

1.	What are the main sources of power consumption in CMOS circuits?	CO1	[K_1]
2.	Why is low-power design important in CMOS technology?	CO1	[K_2]
3.	Write is the role of parallelism in architectural-level voltage scaling.	CO5	[K_2]
4.	What is supply voltage scaling in CMOS circuits?	CO5	[K_1]
5.	Discuss the importance of glitch power in low-power design.	CO2	[K_2]
6.	Describe adiabatic switching circuits and their significance in low-power design.	CO2	[K_2]
7.	How does transistor stacking help in standby leakage reduction?	CO4	[K_2]
8.	Why is dual-Vt (Dual Threshold CMOS) assignment considered an effective approach for leakage reduction?	CO4	[K_2]
9.	In the context of probabilistic power analysis, why might a circuit design that appears to have low average power consumption still cause significant thermal issues?	CO3	[K_2]
10.	Explain the concept of simulation power analysis in the context of power estimation.	CO3	[K_2]

Answer any FIVE Questions:-
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11.	Elucidate the basic principle of low power design in CMOS circuits. Discuss the key techniques used to achieve power efficiency.	CO1	[K_1]

12.	Explicate the concept of dynamic voltage scaling (DVS) and adaptive voltage scaling (AVS). Discuss how these techniques are used to optimize power efficiency in modern digital systems.	CO5	[K$_2$]

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    CO5 [K$_2$]

13. Deliberate advanced low-power techniques for SRAM and DRAM, including state encoding, logic styles, adiabatic switching, and variation-tolerant design.

    CO2 [K$_2$]

14. Examine the various techniques for standby leakage power reduction in CMOS circuits. Illustrate your answer with relevant examples.

    CO4 [K3]

15. Illustrate the concept of logic-level power estimation in digital circuits. Discuss the methodologies used for logic-level power estimation, including dynamic and static power estimation techniques. Provide examples to illustrate each technique.

    CO3 [K1]

16. Explain the various architectural-level optimization techniques for minimizing switched capacitance in digital circuits. Discuss their impact on power consumption and performance.

    CO2 [K$_2$]

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