



B.E/B.TECH DEGREE EXAMINATIONS: NOV/DEC 2024

(Regulation 2018)

Sixth Semester

ELECTRONICS AND COMMUNICATION ENGINEERING

U18ECI6203: VLSI and HDL Programming

COURSE OUTCOMES

CO1: Implement and verify combinational and sequential circuits using Verilog HDL.

CO2: Explain working and electrical properties of MOSFET.

CO3: Discuss the CMOS fabrication Technologies.

CO4: Apply CMOS logics in complex digital circuits.

CO5: Discuss various implementation strategies.

Time: Three Hours

Maximum Marks: 100

Answer all the Questions:-

PART A (10 x 2 = 20 Marks)

(Answer not more than 40 words)

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|--|-----|-------------------|
| 1. Compare and contrast blocking and non-blocking statements. | CO1 | [K ₂] |
| 2. Recall the three types of modeling in Verilog HDL | CO1 | [K ₁] |
| 3. Distinguish Enhancement and depletion type MOSFET | CO2 | [K ₂] |
| 4. Rephrase the concept of channel length modulation | CO2 | [K ₁] |
| 5. List any two mechanisms to avoid latch up in CMOS circuits | CO3 | [K ₁] |
| 6. Define photolithography | CO3 | [K ₁] |
| 7. Make use of static CMOS design style and implement NAND logic | CO4 | [K ₃] |
| 8. Make use of pass transistors and design a NOR logic | CO4 | [K ₃] |
| 9. Define the hardware software nature of SoC | CO5 | [K ₁] |
| 10. Name any two applications of FPGA | CO5 | [K ₁] |

Answer any FIVE Questions:-

PART B (5 x 16 = 80 Marks)

(Answer not more than 400 words)

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|---|----|-----|-------------------|
| 11. Summarize the three types of modeling in Verilog HDL with example Verilog codes for each. | 16 | CO1 | [K ₂] |
|---|----|-----|-------------------|

12.	Explain the working principle and VI graph of N type Enhancement mode MOSFET, deriving the output drain current for cutoff, linear and saturation regions.	16	CO2	[K ₂]
13.	a) Illustrate NMOS fabrication process in detail with neat sketch	10	CO3	[K ₂]
	b) Make use of lambda design rules and draw the stick diagram as well as layout of CMOS Inverter	6	CO3	[K ₃]
14.	Make use of the static CMOS logic design style to implement the following logic.	16	CO4	[K ₃]
	i) Full adder			
	ii) XOR			
15.	Explain the design flow of SoC in detail with a neat flow chart	16	CO5	[K ₂]
16.	Outline the VI characteristics of CMOS inverter and derive the output voltage for all the five regions	16	CO1	[K ₂]
