Register Number:……..

B.E. DEGREE EXAMINATIONS: NOV /DEC 2024

(Regulation 2018)

Fourth Semester

ELECTRICAL AND ELECTRONICS ENGINEERING

U18EEI4203: Digital Electronics

COURSE OUTCOMES

CO1: Understand the operation of basic logic gates and logic families.

CO2: Analyze, Design and Implement various combinational logic circuits.

CO3: Design counters and simple synchronous sequential logic circuits using Flip Flops.

CO4: Classify different semiconductor memories and identify suitable PLD for the applications.

Time: Three Hours **Maximum Marks: 100**

Answer all the Questions: -
PART A (10 x 2 = 20 Marks)
(Answer not more than 40 words)

1.	Convert the binary number 11001.0110_2 to its equivalent decimal number.	CO1	[K_2]
2.	Simplify the Boolean function	CO1	[K_2]
3.	Define carry propagation delay.	CO2	[K_2]
4.	Compare combinational and sequential circuits.	CO2	[K_2]
5.	A 5-bit asynchronous binary counter is made up of five flip-flops, each with a 12 ns propagation delay. The total propagation delay is _____.	CO3	[K_2]
6.	Classify shift registers.	CO3	[K_2]
7.	Differentiate Moore and Mealy model.	CO3	[K_2]
8.	What is race around condition and how it can be eliminated?	CO3	[K_2]
9.	Differentiate RAM & ROM.	CO4	[K_2]
10.	Define noise margin.	CO4	[K_2]

Answer any FIVE Questions: -
PART B (5 x 16 = 80 Marks)
(Answer not more than 400 words)

11.	a)	Simplify the Boolean function using Karnaugh map. F (A, B, C, D) =Σm (0,1,4,5,9,11,14,15) +d (10,13).	10	CO1	[K_3]
	b)	The two binary numbers are A=01100101 & B= 11010101. Perform (i) A-B (ii) B-A using 2's Complement method.	6	CO1	[K_3]
12.	a)	Implement the following Boolean function using 8:1multiplexer: F (A, B, C,D) = ∑m(1,3, 6,7,10,11,13,15)	8	CO2	[K_3]
	b)	Design full subtractor using logic gates.	8	CO2	[K_2]
13.		Design and implement synchronous decade counter using JK flip flop. Draw its timing diagram.	16	CO3	[K_3]
14.	a)	Obtain the reduced state table for the following state table.	8	CO3	[K_3]

Present state	Next state		Output	
	X=0	X=1	X=0	X=1
A	D	A	0	0
B	C	D	1	0
C	C	D	1	0
D	D	B	0	0
E	D	F	0	0
F	D	A	0	0
G	G	F	0	0
H	B	D	1	0

	b)	Describe the procedure for designing synchronous sequential circuits.	8	CO3	[K_2]
15.	a)	Implement the following two Boolean functions with a PLA: F1(A, B, C) = Σ m (0,3,4,7) and F2(A, B, C) = Σ m (3,5,6,7)	10	CO4	[K_2]
	b)	With neat diagram, explain the operation of a CMOS NAND gate.	6	CO4	[K_2]
16.		What is Magnitude Comparator? Design a 2-bit Comparator by writing its Truth Table, Boolean expression, and logic diagram.	16	CO2	[K_3]

****