KUMARAGURU
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M.E./M.TECH DEGREE EXAMINATIONS: NOV/ DEC 2024

(Regulation 2024)

First Semester

EMBEDDED SYSTEMS TECHNOLOGIES

24ETT501: Advanced Digital Design and Reconfigurable Computing

COURSE OUTCOMES

CO1: Design and Analyze Clocked synchronous and sequential circuits for developing simple digital system

CO2: Design and analyze asynchronous sequential circuits in digital system

CO3: Understand the basics and advanced concepts in testing of digital circuits

CO4: Apply the techniques to design synchronous sequential circuit using programmable devices

CO5: Familiarize the basics and processors for reconfigurable computing

Time: Three Hours   **Maximum Marks: 100**

### PART A (4*20 = 80 Marks)

1. Scenario:

   You are tasked with developing a reconfigurable processor-based control system for an electric vehicle's (EV) DC motor. The system must deliver efficient speed control, energy optimization, and fault tolerance while adapting to varying driving conditions such as city traffic, highways, and steep inclines.

   a) Describe the step-by-step design procedure for implementing the DC motor control algorithm on a reconfigurable processor.   6   CO5   [K_4]

   b) Explain the key architectural features of a reconfigurable processor that make it suitable for adaptable DC motor control.   6   CO5   [K_3]

   c) Discuss the significance of using a System-on-Chip (SoC) for this application and its impact on system performance.   6   CO5   [K_3]

   d) Outline recent trends in reconfigurable processors and state their impact on motor control systems.   2   CO5   [K_2]

2. a) Analyse the programming methods of PAL and PLA. How does the programming process affect their functionality and reusability in logic circuit implementation?   6   CO4   [K$_4$]

b) Compare and contrast Programmable Logic Devices (PLD) and Complex Programmable Logic Devices (CPLD)   6   CO4   [K$_2$]

c) Provide an overview of Field-Programmable Gate Arrays (FPGAs), focusing on their working principles and applications. Explain why FPGAs are preferred over CPLDs for high-performance systems.   6   CO4   [K$_2$]

d) How does the Virtex series improve upon the limitations of earlier FPGA models?   2   CO4   [K$_3$]

3. a) Apply D Algorithm to detect 'h', the s-a-0 fault in the below circuit and derive the test vectors.   10   CO3   [K$_3$]
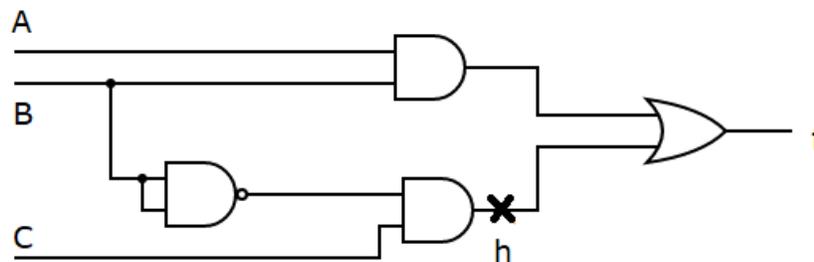
b) What is meant by DFT schemes in digital circuit design? Provide a block diagram of a typical Built-in Self-Test (BIST) architecture and describe the function of its key components.   10   CO3   [K$_3$]

4. a) For the clocked synchronous sequential network shown below, construct the excitation table, transition table, state table and state diagram.   16   CO1   [K$_4$]
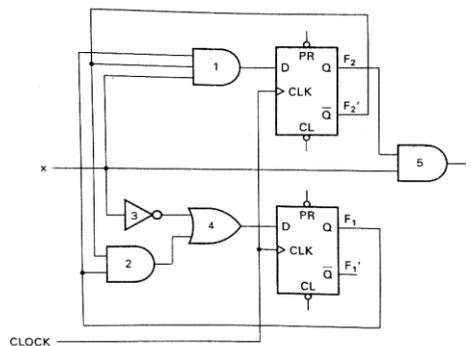
b) Draw an ASM Chart to depict a 3-bit binary counter. 4 CO1 [K₃]

Answer any ONE Question
PART B (1*20 = 20 Marks)

5. a) Using suitable procedure, reduce the below Primitive Flow Table of a fundamental mode Asynchronous Sequential Network. 14 CO2 [K₄]

Present state	Next state				Output (z)			
	Input state (x_1x_2)				Input state (x_1x_2)			
	00	01	10	11	00	01	10	11
A	Ⓐ	B	C	–	0	–	–	–
B	–	Ⓑ	–	D	–	1	–	–
C	E	–	Ⓒ	F	–	–	0	–
D	–	G	C	Ⓓ	–	–	–	0
E	Ⓔ	H	I	–	0	–	–	–
F	–	B	C	Ⓕ	–	–	–	0
G	–	Ⓖ	–	F	–	1	–	–
H	A	Ⓗ	–	–	–	0	–	–
I	A	–	Ⓘ	–	–	–	0	–

b) Explain the occurrence of static, dynamic, and essential hazards in digital systems with examples. 6 CO2 [K₃]

OR

6. a) You are designing a vending machine controller for an automated snack dispenser in a company. The machine accepts Indian coins (1, 2, 5, and 10 rupees) and dispenses snacks when the correct amount is entered. Design a simple state machine for the vending machine controller, including states for accepting coins, checking if the correct amount is paid, and dispensing a snack. 14 CO2 [K₄]

b) Explain the concept of data synchronizers in digital systems. 6 CO2 [K₃]

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